

ABSTRACT OF THE DISCLOSURE

A system for on-chip testing of embedded memories using Address Space Identifier (ASI) bus in Scalable Processor ARChitecture (SPARC) microprocessors. An integrated circuit includes a plurality of memory arrays, Address Space Identifier (ASI) bus interface logic connected by an ASI bus to the plurality of memory arrays, and a memory control unit and a memory built-in self-test (MBIST) engine connected to the ASI bus interface logic. Rather than direct access, the MBIST engine utilizes the ASI bus interface logic and the ASI bus to perform memory testing. The MBIST engine, programmed with memory array parameters, includes a programmable state machine controller to which is connected a programmable data generator, a programmable address generator, and a programmable comparator. The data generator provides data as appropriate. The address generator provides addresses as appropriate. The comparator provides test results information for the particular test situation. The MBIST engine generates a test status output.